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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,860	03/29/2004	Hiroyuki Akatsu	FIS920030415US1	2859

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,860	AKATSU ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 03/20/2006.

Claims 1-10 and 21-28 are active in this application.

Claim(s) 11-20 have been cancelled.

New claim(s) 21-28 have been added.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Corrections to the drawing have been considered and accepted.

Remarks

3. Applicant's arguments filed on 03/20/2006 have been fully considered, but are moot in view of the new ground of rejection.

Withdrawal of Allowability

4. The indicated allowability of claim 2 is withdrawn in view of the newly discovered reference(s) to Hopper et al., US Patent No. 6,964,907. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim(s) 2, 21-23, 27, and 28 are rejected under 35 U. S. C. § 102 (b/e) as being anticipated by U.S. Patent No. 6,964,907 to Hopper et al.

Regarding claim 2, Hopper discloses a bipolar transistor, comprising:

a collector laver 210 (fig. 2);

an intrinsic base laver 206 overlying said collector laver 210;

a low-capacitance region laterally 216 (fig. 2) or 1510/1512 (fig. 16) adjacent to said collector laver including a void 1510/1512 (fig. 16) disposed in an undercut underlying said intrinsic base layer (col. 4, lines 9-23, describes a device similar to the device illustrated by in fig. 2, except that the lateral trenches 1510 and 1512 are filled with air gap instead of with insulating material as lateral trenches 216/218 of fig. 2);

an emitter layer 202 overlying said intrinsic base layer 206; and

a raised extrinsic base layer 208 overlying said intrinsic base laver 206.

Regarding claim 21, Hopper discloses a bipolar transistor wherein said low-capacitance region further includes a solid dielectric region1600, wherein at least one of said void 1510/1512 or said solid dielectric region 1600 contacts said collector layer. See col. 4, lines 9-23.

Regarding claim 22, Hopper discloses the bipolar transistor wherein said intrinsic base layer 206 is laterally surrounded by said solid dielectric region 214/1600.

Regarding claim 23, Hopper discloses the bipolar transistor wherein said raised extrinsic base layer 208 is self-aligned to said emitter layer. 202. See fig. 2.

Regarding claim 27, Hopper discloses the bipolar transistor wherein said intrinsic base layer 206 includes a layer of a single-crystal semiconductor material which forms a heterojunction with a material of at least one of said emitter layer 202 and said collector layer 210. See col. 2, line 10 to col. 3, line 51.

Regarding claim 28, Hopper discloses the bipolar transistor wherein said single-crystal semiconductor material layer included in said intrinsic base layer includes silicon germanium. See col. 2, line 10 to col. 3, line 51.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim(s) 1, 4, 6 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,492,238 to Ahlgren et al.

Regarding claim 1, Ahlgren discloses a bipolar transistor, comprising:

a collector layer 105 (fig. 18);

an intrinsic base layer 190 overlying said collector layer;

a low-capacitance region 110, 120, 160, 170 laterally adjacent to said collector layer including a dielectric region 110, 120, 160, 170 disposed in an undercut directly underlying said intrinsic base layer 190;

an emitter layer 350 overlying said intrinsic base layer 190; and

a raised extrinsic base layer 310 (fig. 17) overlying said intrinsic base layer 190.

It is noted that though Ahlgren does not expressly and specifically discuss about the material of the dielectric region 110, 120, 160, 170, it would have been obvious to one having ordinary skill in the art at the time the invention was made that any suitable well known dielectric material may be used. Silicon dioxide, for example, is a well

known low-capacitance dielectric material that is suitable for use as isolation region (for example, in US Patent No. 5,798,561 to Sato, silicon dioxide is used as dielectric material for isolation regions 4, 6 shown in figs. 3, 5). Hence, it would have been obvious for an ordinary artisan to use silicon dioxide as a material for the low-capacitance region 110, 120, 160, 170 to fulfill the desired function of the device of Ahlgren.

Regarding claim 4, Ahlgren discloses the bipolar transistor wherein said intrinsic base layer 190 is surrounded by said dielectric region 110,120, 160, 170. See fig. 5.

Regarding claim 6, Ahlgren discloses the bipolar transistor wherein said raised extrinsic base layer 310 is spaced from said emitter layer 350 by a first spacer (figs. 16-18) having a sidewall wholly in contact with said raised extrinsic base layer 310 and a second spacer 300 (figs. 11-15) overlying said first spacer, said second spacer having a sidewall wholly in contact with said emitter layer 350.

9. Claim(s) 1, 3, 5-10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,777,302 to Chen et al.

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived

from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Chen discloses a bipolar transistor, comprising:

a collector layer included in substrate 10 (col. 3, line 67 to col. 4,line 5);

an intrinsic base layer 14 overlying said collector layer;

a low-capacitance region 12 laterally adjacent to said collector layer including a dielectric region 12 disposed in an undercut directly underlying said intrinsic base layer 14;

an emitter layer 30 overlying said intrinsic base layer 14; and

a raised extrinsic base layer 22 overlying said intrinsic base layer. See further col. 1, line 60 to col. 2, line 10; col. 4, lines 41-53.

It is noted that though Chen does not expressly and specifically discuss about the material of the dielectric region 12, it would have been obvious to one having ordinary skill in the art at the time the invention was made that any suitable well known dielectric material may be used. Silicon dioxide, for example, is a well known low-capacitance dielectric material that is suitable for use as isolation region (for example, in US Patent No. 5,798,561 to Sato, silicon dioxide is used as dielectric material for isolation regions 4, 6 shown in figs. 3, 5). Hence, it would have been obvious for an ordinary artisan to use silicon dioxide as a material for the low-capacitance region 12 to fulfill the desired function of the device of Chen.

Regarding claim 3, Chen discloses the bipolar transistor wherein said low-capacitance region 12 includes at least one of a void and a solid dielectric region 12 contacting said collector layer. See fig. 2.

Regarding claim 5, Chen discloses the bipolar transistor wherein said raised extrinsic base layer 22 is self-aligned to said emitter layer. See col. 5, lines 5-62.

Regarding claim 6, Chen discloses the bipolar transistor wherein said raised extrinsic base layer 22 is spaced from said emitter layer 30 by a first spacer 16 having a sidewall wholly in contact with said raised extrinsic base layer 22 and a second spacer 28 overlying said first spacer 16, said second spacer 28 having a sidewall wholly in contact with said emitter layer 30. See fig. 7.

Regarding claim 7, Chen discloses the bipolar transistor wherein said collector layer has a dopant concentration of about 10^{20} cm^{-3}. See col. 3, line 61 to col. 4, line 5.

Regarding claim 8, Chen discloses the bipolar transistor further comprising a subcollector disposed below said collector layer, and a trench isolation region surrounding peripheral edges of said subcollector. See col. 3, line 61 to col. 4, line 5.

Regarding claim 9, Chen disclose the bipolar transistor wherein said intrinsic base layer 14 includes a layer of a single-crystal semiconductor material which forms a

heterojunction with a material of at least one of said emitter layer and said collector layer. See col. 4, lines 6-53; col. 6, lines 7-58.

Regarding claim 10, Chen discloses the bipolar transistor wherein said single-crystal semiconductor material layer included in said intrinsic base layer includes silicon germanium. See col. 4, lines 6-53; col. 6, lines 7-58.

10. Claim(s) 24-26 are rejected under 35 U.S.C. 103 (a) as being unpatentable over by U.S. Patent No. 6,964,907 to Hopper et al., in view of Verma et al., U.S. Patent No. 7,022,578.

Regarding claims 24 and 26, Hopper discloses the bipolar transistor comprising all claimed limitations, except for explicitly discussing about the raised extrinsic base layer being spaced from said emitter layer by a first spacer having a sidewall wholly in contact with said raised extrinsic base layer and a second spacer overlying said first spacer, said second spacer having a sidewall wholly in contact with said emitter layer, nor about a subcollector disposed below said collector layer, and a trench isolation region surrounding peripheral edges of said subcollector.

Verma discloses a bipolar transistor comprising collector 1014 and subscollector 1004 (figs. 15), disposed below the collector 1014, trench isolation region 1008/1010 surrounding peripheral edges of the collector/subcollector, intrinsic base 1304, emitter 1400, raised extrinsic base 1506; wherein the raised extrinsic base 1506 being spaced

from said emitter layer 1400 by a first spacer 1402 having a sidewall wholly in contact with said raised extrinsic base layer 1506 and a second spacer 1404 overlying said first spacer 1402, said second spacer 1404 having a sidewall wholly in contact with said emitter layer 1400.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further including spacers and subcollector as those of Verma into the invention of Hopper in order to fulfill the desired function of the device of Hopper to obtain a bipolar transistor with enhanced performance (see col. 4, lines 28-31 of Verma).

11. Claim(s) 25 are rejected under 35 U.S.C. 103 (a) as being unpatentable over by U.S. Patent No. 6,964,907 to Hopper et al.

Regarding claim 25, Hopper discloses the bipolar transistor comprising all claimed limitations, except for expressly discussing about the collector layer having a dopant concentration of about 10^{20} cm^{-3}.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the dopant concentration of the collector can be at any suitable value, depending on the desired device. Modification of the device of Hopper so that the collector layer having a desired dopant concentration would involve only routine skills in the art.

Conclusion

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571)272-1907. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

ANDY HUYNH
PRIMARY EXAMINER

Dao H. Nguyen
Art Unit 2818
June 2, 2006

Accepted
DN
06/01/06

FIG. 1
Prior Art

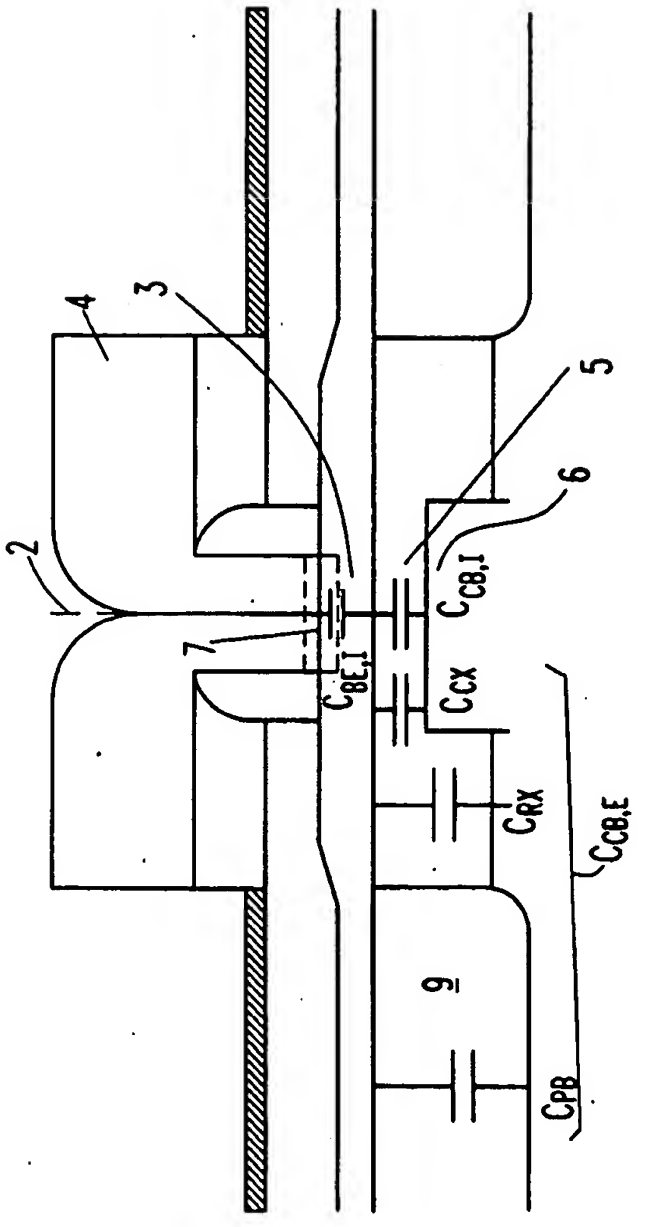

FIG. 2
Prior Art